data located anywhere in said information array, said repairing data for identifying and repairing defective columns or rows comprising said main memory array despite corruption of the repairing data as read

~~enabling said error correction coding circuit during an access of said main array for correcting a correctable error if a particular address corresponds to an address of at least one defective column, wherein said particular address comprises a Y-address~~.

9. (currently amended) A method for improving repairing efficiency in a non-volatile memory, said method comprising the steps of:

reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory, wherein said column repair data is read utilizing a read circuit linked to a main memory array ~~associated with~~ comprising said non-volatile memory and an error correction coding circuit separate from said information array linked to said volatile latch array and thereby to a decoder circuit, said information array sharing

said read circuit with said main memory array;

~~providing a plurality of columns and rows associated with said non-volatile memory;~~

~~associating each of said plurality of columns associated with said non-volatile memory with a respective I/O terminal;~~

~~associating a spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and~~

enabling said error correction coding circuit during reading of said repairing data including corrupted repairing data located anywhere in said information array to thereby identify and repair defective columns or rows ~~associated with~~ comprising said ~~non-volatile memory~~ main memory array despite corruption of the repairing data as read; and,

enabling said error correction coding circuit during an access of said main memory array for correcting a correctable error if a particular address corresponds to an address of at least one defective column comprising said main memory array,

wherein said particular address comprises a Y-address.

10. (canceled)

11. (currently amended) A system for improving repairing efficiency in a non-volatile memory, said system comprising:

a reading circuit for reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory, said information array sharing said read circuit with a main memory array comprising said non-volatile memory; and,

~~a plurality of columns and rows each associated with said non-volatile memory, wherein each of said plurality of associated columns and rows is further associated with a respective I/O terminal;~~

~~a spare column associated with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and~~

an error correction coding circuit separate from said

information array adapted to be enabled during reading of said repairing data including reading corrupted repairing data located anywhere in said information array, said repairing data for identifying and repairing defective columns or rows ~~associated with~~ comprising said ~~non-volatile memory~~ main memory array despite corruption of the repairing data as read.

12. (currently amended) The system of claim 11 ~~further comprising~~ wherein:

said error correction coding circuit is adapted to be enabled during an access of a main memory array ~~associated with~~ comprising said non-volatile memory for correcting a correctable error if a particular address corresponds to an address of at least one defective column.

13. (previously presented) The system of claim 12 wherein said particular address comprises a Y-address corresponding to said at least one defective column.

14. (currently amended) The system of claim 11 further wherein

said read circuit is linked to said main array to thereby permit data to be read from said main memory array and to be transmitted to said error correction coding circuit;

said error control circuit is connected to said volatile latch array to thereby permit data to be transferred from said error correction coding circuit to said volatile latch array; and

said error correction coding circuit is linked to a decoder circuit, and thereby to said information array, at least one spare row, and said main memory array, said main memory array includes a normal array and at least one spare column.

15. (previously presented) The system of claim 14 further wherein said volatile latch array is linked to said decoder circuit to thereby permit data contained within said volatile latch array to be accessed by said decoder circuit.

16. (currently amended) The system of claim 11 wherein:

said repairing data contained within said information array is accessed following initialization of a computer system associated with said volatile latch array, thereby resulting in

the transfer of said repairing data to said ~~non-volatile memory~~ volatile latch array.

17. (currently amended) A system for improving repairing efficiency in a non-volatile memory, said system comprising:

a read circuit for reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory, said information array sharing said read circuit with a main memory array comprising said non-volatile memory; and,

~~providing a plurality of columns and rows associated with said non-volatile memory;~~

~~associating each of said plurality of columns associated with said non-volatile memory with a respective I/O terminal;~~

~~associating a spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and~~

an error correction coding circuit separate from said information array adapted to be enabled during reading of said

repairing data including reading corrupted repairing data located anywhere in said information array, said repairing data for identifying and repairing defective columns or rows comprising said main memory array despite corruption of the repairing data as read;

[[an]] said error correction coding circuit enabled during an access of a main memory array ~~associated with~~ comprising said non-volatile memory for correcting a correctable error if a particular address corresponds to an address of at least one defective column comprising said main memory array, wherein said particular address comprises a Y-address.

18. (currently amended) A system for improving repairing efficiency in a non-volatile memory, said system comprising:

a read circuit for reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory, wherein said read circuit is linked to a main memory array ~~associated with~~ comprising said non-volatile memory and an error correction coding circuit separate from said information array

linked to said volatile latch array and thereby to a decoder circuit, said information array sharing said read circuit with said main memory array;

~~providing a plurality of columns and rows associated with said non-volatile memory;~~

~~associating each of said plurality of columns associated with said non-volatile memory with a respective I/O terminal;~~

~~associating a spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and~~

wherein said error correction coding circuit is adapted to be enabled during reading of said repairing data including reading corrupted repairing data located anywhere in said information array, said repairing data for identifying and repairing defective columns or rows comprising said main memory array despite corruption of the repairing data as read;

~~wherein said error correction coding circuit is enabled during an access of said main array for correcting a correctable~~

~~error if a particular address corresponds to an address of at least one defective column, wherein said particular address comprises a Y-address~~.

19. (currently amended) A system for improving repairing efficiency in a non-volatile memory, said system comprising:

a read circuit for reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory, wherein said read circuit is linked to a main memory array ~~associated with~~ comprising said non-volatile memory and an error correction coding circuit separate from said information array linked to said volatile latch array and thereby to a decoder circuit, said information array sharing said read circuit with said main memory array;

a plurality of columns and rows each associated with said non-volatile memory, wherein each of said plurality of associated columns and rows is further associated with a respective I/O terminal;

a spare column associated with at least two of each of said

plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and

wherein said error correction coding circuit is adapted to be enabled during reading of said repairing data including reading corrupted repairing data located anywhere in said information array, said repairing data for identifying and repairing defective columns or rows ~~associated with comprising said non volatile memory~~ comprising said main memory array despite corruption of the repairing data as read;

wherein said error correction coding circuit is adapted to be enabled during an access of said main memory array for correcting a correctable error if a particular address corresponds to an address of at least one defective column comprising said main memory array, wherein said particular address comprises a Y-address.

20. (canceled)

21. (currently amended) The method of claim [[1]] 24 further comprising the step of:

using a (16,11) Hamming code to associate said at least one spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal.

22. (canceled)

23. (previously presented) The method of claim 1 further comprising the step of:

enabling the error correction coding circuit unconditionally when accessing an information row within said information array to make certain that said repairing data will be correctly obtained.

24. (new) The method of claim 1, further comprising the steps of:

providing a plurality of columns and rows associated with said non-volatile memory;

associating each of said plurality of columns associated with said non-volatile memory with a respective I/O terminal;

associating at least one spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal.

25. (new) The system of claim 11, further comprising:

a plurality of columns and rows each associated with said non-volatile memory, wherein each of said plurality of associated columns and rows is further associated with a respective I/O terminal; and,

a spare column associated with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal.